UltraCAD Design, Inc.

DESIGN NOTE

ADJUSTING SIGNAL TIMING

Today's high speed logic circuits present several difficult design problems for engineers. Fast rise times lead to bandwidths where circuit board traces become transmission lines, often with unpredictable intrinsic impedance characteristics. Noise margins are reduced by reflections, circuit propagation delays, and noise from adjacent traces (and even from outside the system itself). The **timing** of signals at specific points on the circuit board also becomes a critical issue in the reliability of circuits, and we see some of our customers trying to control signal timing within picoseconds. In this design note, we discuss some of the factors to consider when adjusting signal timing on printed circuit boards.

Theoretical Propagation Delay

Standard reference sources (Motorola's MECL System Design Handbook, for example) give several formulas that relate to the propagation delay of a signal along a trace on a circuit board. These formulas have been combined and summarized in Figure 1. The first part of the formula provides the basic propagation time under unloaded conditions. In that formula, a = 1 and b = 0 for Stripline configurations and a = .475 and b = .67 for Microstrip.

The second part of the formula provides for the slowing of signals due to the capacitive loading along the line. This capacitive loading is caused by the circuit loads on the line and stray, parasitic capacitances.

It is often the case that the propagation delay along a trace is more significant than the signal delay through a component.

$$t_{pd} = 1.017 \sqrt{a\varepsilon_r + b} \sqrt{1 + \frac{C_d}{C_o * l}}$$

Where:
- t_{pd} = Propagation time along trace, in ns/ft
- ε_r = Relative dielectric coefficient
- C_d = Capacitance due to device loads
- C_o = Intrinsic capacitance/unit length
- l = Length of the trace
- a = 1, b = 0 for Stripline
- a = .475, b = .67 for Microstrip

Formula For Propagation Delay Along a Trace
Figure 1

In space, electromagnetic waves travel at the speed of light. On circuit boards signals travel at approximately half that speed. People tend to use 2 ns/ft as a standard rule of thumb when designing circuits. But in fact this figure might be off by as much as 50%, depending on design specifics.

The first important variable in this equation is ε_r, the relative dielectric coefficient. People often use a value of 4.2 for standard FR-4 board material. Actual values can easily range from 4.0 to 4.4 (or more) in the real world, and ε_r even varies *within* a layer as a result of temperature and pressure effects during fabrication. This range results in an uncertainty of t_{pd} of approximately 5%, or about .1 ns/ft. That's 8.3 Psec/in., or 100 Psec in a 12 inch line.

The second important factor is C_d, the sum of the capacitance effects of the loads on the line. A fanout of 8 loads of about 5pf each on a 12 inch line can slow t_{pd} by as much as 50% (1 ns/ft or 83 Psec/in). The calculation of the exact amount requires a calculation of C_o, which itself depends on ε_r and the board interlayer geometries.

The bottom line is that before the delay along a line can be adjusted accurately to meet circuit needs, the actual t_{pd} along the line must be known. The actual tpd along the line depends, among other things, on the design the PCB designer is going to create (i.e. the path lengths) and the processes the board fabricator is going to use.

As board designers, *UltraCAD* can trim a line length as close as a one mil. This is within a fraction of a Psec. Since, in practice, the uncertainty of t_{pd} is as much as 80 Psec in an inch, design tolerances can be almost two orders of magnitude tighter than other sources of uncertainty!

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So what does the circuit design engineer do? First, understand the limitations of accurately estimating t_{pd} before we begin to adjust signal delay times by adjusting line lengths. Then, allow us to work closely with you and the board house who will fabricate the boards. We have found that only a small fraction of board houses really understand these concepts and their processes well enough to help their customers meet very tight requirements. If yours can't, we can help you select one. The cost will not be any higher (neither we nor the board houses charge for such cooperation --- in fact we all enjoy working with customers who design their circuits so carefully), but be sure to allow extra project time to do it right!

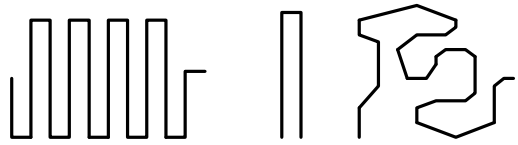
Limits on adjustments

There is a lower limit on propagation time. It's hard to make a trace shorter than the straight line connecting two points! But you can add time to a trace by increasing its length. Conceptually, there is no limit to how much time you can add (up to available surface area!).

UltraCAD can adjust an individual line (or match a differential pair of lines) as close as one mil (.001) without much difficulty. That's about .2 Psec. Although we can adjust lengths even tighter than this, The benefits are seldom worth the effort.

How to route trace lengths

Figure 2 illustrates three alternative ways a trace may be routed to add propagation time to a signal line. We have pointed out in other Design Notes why alternative (b) is undesirable --- it looks just like an antenna. Alternative (a) is even worse! It looks like a dish antenna. The preferred way to add propagation time to a trace is illustrated in (c), a randomly routed line. It is often a good idea to "guard band" such a trace to control cross-talk with other traces and and to minimize susceptibility to radiated energy into the trace.



Alternative Ways To Route Traces To Add Propagation Time To A Line
Figure 2

UltraCAD Design, Inc. is the industry expert when it comes to designing large, complex circuit boards for maximum performance and minimum EMI problems. We routinely design to the highest standards on all boards we do. That's why 80% of our business is with repeat customers. If you are tired of working with service providers who don't understand your requirements, give *UltraCAD* a try. Then, you too will join our list of satisfied customers.

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