UltraCAD Design, Inc.

DESIGN NOTE

CONTROLLING IMPEDANCE

By now, our position that high speed design rules need to be considered in today's designs because of fast rise times should be pretty clear. That means, like it or not (or even if you are aware of it or not) the traces on a PC board will exhibit characteristics of transmission lines. Therefore, the impedance characteristics of those lines need to be considered.

The common formulas for impedance are complex:

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{.8w + t}\right)$$ for microstrip, and

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9(2h + t)}{(.8w + t)}\right)$$ for stripline

Good board fabrication houses will tell you that there are some problems with these equations. First, they are approximations. They are pretty good approximations for microstrip and stripline, but the commonly used rules for dual stripline and for buried microstrip are much less precise. Secondly, they depend heavily on ε_r, the relative dielectric constant. This value varies from manufacturer to manufacturer, and it can even vary within a layer as a function of the pressures and temperatures used in the buildup of the board. Thus, hitting and holding an exact absolute value of Z_0 in a board design and over the life of the design is difficult.

If absolute values of impedance are important in your design, we urge you to get the board designer and the fabrication house "on board" early in the design stage. The board house will already know what the impedance tradeoffs will be for their processes, and will be able to give good advice regarding impedances and propagation times on individual layers as the design progresses. If your board house can't do this, get another board house on board!

But, on the other hand, it may not be the absolute value of the impedance we need to worry about, anyway. IC devices on a board are relatively tolerant of the intrinsic impedances of the traces they interface with. And the impedance will also change as a function of the number of and type of devices on the trace. What is really more important is terminating lines properly (at **whatever** the intrinsic impedance is) and minimizing reflections that result from impedance mismatches, device loading, and stubs at various points on the board.

The above paragraph is true for boards taken by themselves. However, when circuit cards interface with other cards through a backplane, which itself may have impedance controlled traces, holding absolute values of impedance is much more important.

There are some things that do not have much of an effect on trace impedance. One of them is corners (see our Technical Note "RIGHT ANGLE CORNERS"). There are almost no reflections that occur as a result of traces rounding corners. Another is vias. Although there is a geometric discontinuity at a via, it is relatively small and of very short duration, so most investigations have found them to be negligible.

On the other hand, branches in traces can create impedance mismatches on the order of 50%. Consider the situations shown in Figure 1. Assume all the traces are 50Ω. In case (a) the two branches at 50Ω each will parallel to 25Ω. The trace extending from the gate will be 50Ω. So there is a step function transition from 50Ω to 25Ω at the branch. In case (b), however, the branch occurs right at the gate. Thus, the gate sees 25Ω without any significant discontinuity. Since most ICs are relatively tolerant of a wide range in load impedance, this circuit will perform much better than (a). The design rule would be that as long as the branch is within a distance from the gate equal to the rise time of the signal, the circuit should perform reasonably well.

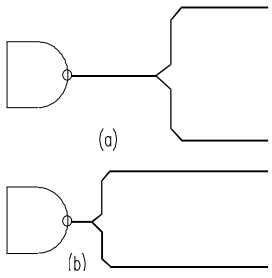

Figure 1

In really critical situations, the trace impedances could be adjusted so that they do match at the branch. Since the

intrinsic impedance is a function of trace width and therefore can be set by changing the width, the impedance of the trace from the gate in (a) could be set to 50% of the intrinsic impedance of the traces after the branch, thus eliminating the impedance mismatch.

There is one other problem in trace routing one rarely sees discussed. Think of a coaxial transmission line. It is a signal line whose geometric relationship to ground is well defined and controlled (as in Figure 2(a)). Although we rarely see it done this way, a coaxial cable would be equally effective if the shield were attached to V_{CC} (as in Figure 2(b)) --- as long as V_{CC} was well regulated and there was a low impedance ac path between ground and V_{CC}. But now if someone spliced a signal line between two coaxial cables such that part of the length was reference to ground and part of it was referenced to V_{CC} (as in Figure 2(c)), we would question the wisdom of such a move.

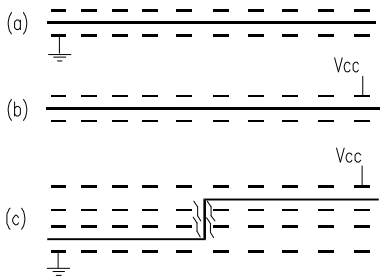

Figure 2

On a PC board, the impedance of a trace is defined by its geometric relationship to one of the power distribution planes. When we assume that the results are the same whether we are defining the relationship to the ground plane or to the power plane, we are implicitly assuming that the ac impedance between the planes is very low --- which is normally a pretty good assumption. There are two times, however, when the assumption is not so good:

(a) When we are dealing with such very high rise times that the inherent inductance of the planes comes into play, and

(b) when we arbitrarily transition the reference from one plane to another (as we might do when we move a signal through a via to another layer) as suggested in Figure 2(c).

In Technical Note T001 (Square Waves, Pulse Rise Times, and Frequencies) we point out that with very high frequencies (harmonics) the RETURN signal tends to flow directly under the signal line on one of the power distribution planes. But if the signal trace transitions from one layer to another so that it becomes referenced to a different distribution plane, the return path is no longer so well defined. In such a case, the return path may transition between ground planes through a through hole device or connector pin that is grounded. Or it may pass through a by pass capacitor from a ground to a power plane. The path can be unpredictable and may become a source of EMI radiation that defies identification.

This can be illustrated by looking at the equivalent circuit of a transmission line on a single layer and one that transitions to another layer (Figure 3) The additional components on the return line (b) reflect the impact of the via. The impact would be minimal for traces that simply transition on opposite sides of the same reference layer. It would become greater for traces that move to different reference planes and are farther away from alternative paths for their return signals.

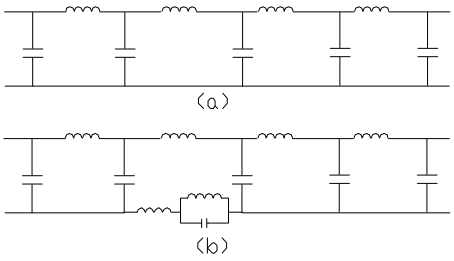

Figure 3

This is not to say that signal lines should not be allowed to transition from one layer to another. But it is to say that in very critical systems this is one of many design characteristics that must be considered. Service Bureaus that do not understand this may inadvertently get their customers in trouble!

In summary: Impedance calculations are very complex and depend on variables (principally ε_r) that are difficult to control. Fortunately, most applications require **constant** impedance traces, but not necessarily traces with exact absolute values of impedance (except when interfaces with backplanes and other circuit cards are required.) Stubs and "Y's" can have significant effects and must be carefully controlled to avoid reflections due to step function changes in impedance. Turns and vias generally have minimal effect on impedance, except that moving a controlled impedance trace from one layer to another can cause significant and subtle problems unless the two layers are on immediately opposite sides of a single power distribution (reference) plane.