UltraCAD Design, Inc.

DESIGN NOTE

TRANSMISSION LINE ISSUES

PCB Structures:

Transmission lines consist of a (signal) wire(s) placed in a defined relationship with a ground plane. A coaxial cable is a common example of such a transmission line. In general, there are five types of printed circuit board structures that need to be considered when looking at transmission line issues:

Microstrip
Buried (or Embedded) Microstrip
Stripline
Dual Stripline
Unbalanced Stripline.

Figure 1 illustrates the three most common of these.

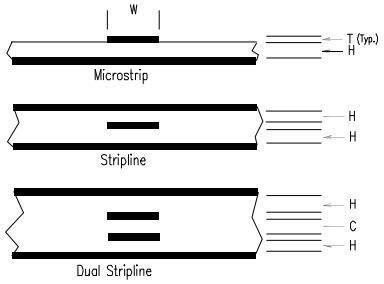

Figure 1

Three Typical PC Board Structures

Microstrip refers to a typical trace on the "surface" of a PCB that is placed over a power or ground plane. Buried, or embedded, microstrip refers to a similar structure, but one which is covered with a coating, such as a conformal coating. The effect of the coating is hard to estimate, but it is a function of the thickness of the coating and the relative dielectric coefficient of the coating material.

Stripline refers to a trace placed (typically symmetrically) between two power distribution planes. Dual stripline refers to a similar structure with two trace layers between the planes. Unbalanced stripline configurations would have two or more signal layers between the planes in structures that may not be symmetrical.

There are formulas (See out Technical notes on Controlling Impedance and Controlling Signal Timing) for intrinsic impedance and propagation delay as a function of the type of structure. None of them are truly precise. They are reasonably accurate for microstrip and stripline, but become much less accurate for other structures. Therefore, some people resort to using "rules of thumb" for adjusting the formulas in the other configurations. A **good** board fabrication house will have run studies on these various configurations, based on their own particular manufacturing processes, and can help their customers calculate precise values when necessary. But many board houses don't have the interest or knowledge for doing this. Therefore, *UltraCAD* always recommends that our customers pick their board fabricators **early** in the design process and bring them on the team well **before** it's time for the actual fabrication.

Typical Guidelines:

Many circuit designers are uncertain about when they need to incorporate high speed design rules into their printed circuit board specifications. High speed design rules begin to be important when the high frequency components of the signals reach sufficiently high levels. The problem is that "how high is high?" is not clearly defined. One writer argues that **all** frequencies are high enough for logic families used in today's systems. We often point out that the thresholds can be surprisingly low, since the critical issue is RISE TIME, not frequency. This note discusses the generally accepted guideline, the problems with it, and *UltraCAD*'s approach to high performance designs.

One of the primary factors in determining when it is necessary to treat printed circuit board traces as transmission lines is the rise time (AND the FALL time) of the signals on the line. Standard guidelines suggest that one should use transmission line design factors if "the two way delay of the line is less than the rise time of the pulse," or:

$$\text{if the line length} > t_r / 2t_{pd}$$

where t_r is the rise time of the pulse and t_{pd} is the propagation delay of one inch of line. But this rule is not as safe as it might sound.

Guideline Problems:

1. This is not the length of line at which there is **no** effect. It is the length at which the effect is "tolerable" under some definition and some set of conditions. For MECL logic (according to Motorola) it is the point at which the resultant undershoot and ring are "held to about 15% of the logic swing." And that is if one considers only the effect of one device and one trace by itself and not in interaction with other possible noise sources.

   Some designers fall into the trap of thinking that designs are "good" or "bad". Actually designs are "better" or "worse", and you may not find out about yours until well after the prototype stage. The worst design to have is one that works MOST of the time. It's the infrequent, random times that it doesn't work that causes maddening troubleshooting efforts and irate customers.

   We've found that good designers don't design to "acceptable" levels of noise immunity and margin. They design for the maximum possible noise margin, and in doing so they tend to have the fewest number of subsequent problems.

2. The propagation time is itself a complex function of many factors including ε_r, loading, intrinsic impedance, and type of board construction (microstrip or stripline). Again, referencing Motorola's guidelines for typical MECL 10KH gates, the maximum "tolerable" line length can vary as much as 300% as follows:

   3.5" for microstrip if $Z_o = 50\,\Omega$ and fanout = 1

   1.0" for stripline if $Z_o = 50\,\Omega$ and fanout = 8

3. Designers may assume that this issue only arises for ECL circuits, which is why very stringent PCB routing is sometimes called "ECL routing". But other types of logic may also need special consideration when routing:

   "Transmission line effects, at the PC board or motherboard level, were of little concern with the older, slower TTL and CMOS families....However when advanced Schottky, advanced CMOS, ECL or GaAs devices ... are used, transmission-line effects *are of concern at the PC board level.* ***For all practical purposes, all signal lines are transmission lines when today's logic components are used to implement digital designs***." (emphasis added)

   (Quoted from Computer Engineering Handbook, McGraw Hill, 1992, p. 7.27)

   More than one company has found that their designs performed acceptably until they changed chip suppliers or the chip supplier "improved" the product with a faster rise time! It takes a long time to figure out why a good design suddenly turned marginal!

Design Steps:

We recommend as a minimum the following steps be taken in the design process.

1. Determine if transmission line routing seems prudent for the circuit and components (remember the issue is related to both rise AND fall times of the logic used). In view of the practical problems associated with using the standard design rule, we'd recommend one that is more conservative by a factor of five:

   $$\text{If the line length} > .1 * (t_r / t_{pd})$$

2. If transmission line routing might be an issue, address the question of transmission line termination and load (e.g. whether series, parallel, or Thevenin equivalent loading will be used). Ignoring termination and loading issues can result in poor reliability later.

3. If series termination is selected, use extreme care with stub and distributed load routing (because of the effect of the reflected signal from the far end of the transmission line.)

4. Also use care with stub and distributed load routing if parallel (load) termination is used. Each load adds some capacitance, and that capacitance (a) lowers the intrinsic impedance of the line, (b)

slows down the signal propagation delay down the line, and (c) causes at least some reflection at the line.

If transmission line routing seems prudent, the generally accepted design rule for maximum stub length is the same as described above. In consideration of the problems addressed above, however, ***UltraCAD*'s design rule is to design for absolute minimum stub length.** What we usually achieve is ZERO stub length. We can **always** route to 3/16 inch stub length even in the tightest circumstances (such as when pin escape stringers are needed for SMT components).

We achieve this goal through a four-stage design strategy.

(a) We spend a great deal of time planning for and optimizing the placement of parts. We believe we are the best in the country at placement, and in fact have put on seminars for some customers on this topic. Our placements are a big part of the reason for the improved routing and performance that our customer's PC boards enjoy.

(b) Then we manually route all critical clock and logic paths, making sure loading and propagation delays are **exactly** what you want.

UltraCAD routinely works with our customers in matching and controlling propagation times down a line. We can match differential signal pairs almost exactly (within picoseconds). Other lines can be matched within the precision allowed by the estimates of ε_r and capacitive loading assumptions.

(c) Only after we "lock" those traces in do we use the autorouter to put in the non-critical traces.

(d) Finally, we manually clean up the final details of the total, overall routing.

5. If a customer wishes, we can help "trim" the intrinsic impedance of a line (by changing its width) to adjust for uneven loading and can design "splits" in the line (e.g. stubbing two 100Ω parallel lines onto the end of a 50Ω line) to help with particularly difficult routing problems.